What is claimed is:

1. A method for forming a top metalization system for high performance integrated circuits, comprising:

forming an integrated circuit comprising a plurality of devices formed in and on a semiconductor substrate, with an overlaying interconnecting metalization structure connected to said devices and comprising a plurality of first metal lines in one or more layers;

depositing a passivation layer over said interconnecting metalization structure;

depositing an insulating, separating layer over said passivation layer that is substantially thicker than said passivation layer;

forming openings through said insulating, separating layer and said passivation layer to expose upper metal portions of said overlaying interconnecting metalization structure;

depositing metal contacts in said openings; and

forming said top metalization system connected to said overlaying interconnecting metalization structure, wherein said top metalization system comprises a plurality of top metal lines, in one or more layers, each of said top metal lines having a width substantially greater than said first metal lines.

2. The method of claim 1 wherein the top metalization system connects portions of said interconnecting metalization structure to other portions of said interconnecting metalization structure.

3. The method of claim 1 wherein said top metalization system comprises signal lines that are substantially wider than lines in said interconnecting metalization structure.

4. The method of claim 1 wherein said top metalization system comprises power planes having power buses that are substantially wider than lines in said interconnecting metalization structure.

5. The method of claim 1 wherein said top metalization system comprises ground planes having ground buses that are substantially wider than lines in said interconnecting metalization structure.

6. The method of claim 1 wherein said top metalization system comprises planes that contain both signal lines and power buses that are substantially wider than lines in said interconnecting metalization structure.

7. The method of claim 1 wherein said top metalization system comprises planes that contain both signal lines and ground buses that are substantially wider than lines in said interconnecting metalization structure.

8. The method of claim 1 wherein said top metalization system comprises planes that contain both power buses and ground buses that are substantially wider than lines in said interconnecting metalization structure.

9. The method of claim 1 wherein said overlaying interconnecting metalization structure comprises electrical contact points.

10. The method of claim 9 wherein the size of said contact points is within the range of approximately 0.3 um. to 5.0 um.

11. The method of claim 1 wherein said passivation layer comprises Plasma Enhanced CVD (PECVD) oxide.

12. The method of claim 1 wherein said passivation layer comprises Plasma Enhanced CVD (PECVD) nitride.

13. The method of claim 1 wherein said passivation layer comprises a layer within the range of approximately 0.15 to 2.0

um of Plasma Enhanced CVD (PECVD) oxide over which a layer within the range of approximately 0.5 to 2.0 um PECVD nitride is deposited.

14. The method of claim 1 wherein said insulating, separating layer is a polymer dielectric layer or any other appropriate insulating material.

15. The method of claim 1 wherein said insulating, separating layer comprises polyimide.

16. The method of claim 1 wherein said insulating, separating layer comprises the polymer benzocyclobutene (BCB).

17. The method of claim 1 wherein said insulating, separating layer is of a thickness after curing within the range of approximately 1.0 to 30 um.

18. The method of claim 1 wherein said insulating, separating layer is spin-on coated and cured.

19. The method of claim 1 wherein said insulating, separating layer after said spin-on coating is cured at a temperature within the range of approximately 250 to 450 degrees C. for a time

within the range of approximately 0.5 to 1.5 hours said curing to occur within a vacuum or nitrogen ambient.

20. The method of claim 16 wherein said insulating, separating layer is subjected to multiple processing steps of spin on coating and curing.

21. The method of claim 20 wherein said insulating, separating layer after each process step of said spin on coating is cured at a temperature within the range of approximately 250 to 450 degrees C. for a time within the range of approximately 0.5 to 1.5 hours said curing the occur within a vacuum or nitrogen ambient.

22. The method of claim 1 wherein said openings have an aspect ratio within the range of approximately 1 to 10.

23. The method of claim 1 wherein said metal contacts are selected from a group comprise sputtered aluminum, CVD tungsten, CVD copper, electroplated copper and electroless nickel.

24. The method of claim 1 wherein said metal contacts comprise damascene metal filling.

25. The method of claim 1 wherein said top metalization system comprises contact pads on the top metal layer whereby said contact pad can comprise any appropriate contact material, such as but not limited to tungsten, chromium, copper (electroplated or electroless), aluminum, polysilicon, or the like.

26. The method of claim 1 wherein said top metal layer comprises contact pads, said contact pads comprising signal connection pads whereby said signal connection pads can comprise any appropriate contact material, such as but not limited to tungsten, chromium, copper (electroplated or electroless), aluminum, polysilicon, or the like.

27. The method of claim 1 wherein said top metalization system contains contact pads on the top metal layer, said contact pads containing signal connection pads in addition to power and ground connection pads whereby said signal connection pads can comprise any appropriate contact material, such as but not limited to tungsten, chromium, copper (electroplated or electroless), aluminum, polysilicon, or the like.

28. The method of claim 27 wherein said signal pads are mounted in the periphery of said top metalization system and said power and ground connection pads are mounted within the area enclosed

by said signal pads whereby said power and ground connection pads and said signal pads can comprise any appropriate contact material, such as but not limited to tungsten, chromium, copper (electroplated or electroless), aluminum, polysilicon, or the like.

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29. A semiconductor device structure comprising:
a semiconductor substrate comprising semiconductor devices;
an interconnecting metalization structure connected to said devices;
electrical contact points on an upper top surface of said interconnecting metalization structure and connected to said interconnecting metalization structure;
a passivation layer deposited over said interconnecting metalization structure and over said electrical contact points;
an insulating layer deposited over said passivation layer said insulating layer being substantially thicker than said passivation layer;
openings through said insulating layer and through said passivation layer down to the upper surface of said electrical contact points;
metal conductors within said openings; and
an upper metalization structure connected to said metal conductors.

30. The method of claim 29 wherein the upper metalization structure connects portions of said interconnecting metalization structure to other portions of said interconnecting metalization structure.

31. The structure of claim 29 wherein said upper metalization structure further comprises:
a plurality of insulating layers;
a plurality of structures of metal interconnecting lines formed between said insulating layers;
a plurality of contact pads in an upper layer of said metalization structure; and
a plurality of filled openings connecting said contact pads with one or more of said structures of metal interconnecting lines further connecting said contact pads with said electrical contact points.

32. The structure of claim 31 whereby said metal interconnecting lines are signal lines, and are substantially wider than lines in said interconnecting metalization structure.

33. The structure of claim 31 wherein said metal interconnecting lines are power buses, and are substantially wider than lines in said interconnecting metalization structure.

34. The structure of claim 31 wherein said metal interconnecting lines are ground buses, and are substantially wider than lines in said interconnecting metalization structure.

35. The structure of claim 31 wherein said metal interconnecting lines are a combination of signal lines and power buses, and are substantially wider than lines in said interconnecting metalization structure.

36. The structure of claim 31 wherein said metal interconnecting lines are a combination of power and ground buses, and are substantially wider than lines in said interconnecting metalization structure.

37. The structure of claim 31 wherein said metal interconnecting lines are a combination of signal and ground buses, and are substantially wider than lines in said interconnecting metalization structure.

38. The structure of claim 29 wherein the size of said contact points is within the range of approximately 0.3 um. to 5.0 um whereby further whereby said contact points can comprise any appropriate contact material, such as but not limited to

tungsten, copper (electroplated or electroless), aluminum, polysilicon, or the like.

39. The structure of claim 29 wherein said passivation layer comprises a layer within the range of approximately 0.15 to 2.0 um Plasma Enhanced CVD (PECVD) oxide over which a layer within the range of approximately 0.5 to 2.0 um PECVD nitride is deposited.

40. The method of claim 29 wherein said insulating, separating layer is a polymer dielectric layer or any other appropriate insulating material.

41. The method of claim 29 wherein said insulating, separating layer comprises polyimide.

42. The method of claim 29 wherein said insulating, separating layer comprises the polymer benzocyclobutene (BCB).

43. The structure of claim 29 wherein said insulating layer is of a thickness after curing within the range of approximately 1.0 to 30 um.

44. The structure of claim 29 wherein said openings have an aspect ratio within the range of approximately 1 to 10.

45. The method of claim 29 wherein said metal conductors within said openings through said insulating layer and through said passivation layer connecting said electrical contact pads of said top metalization structure with contact points of said interconnecting metalization structure are constructed and routed such that each said electrical contact point of said interconnecting metalization structure is connected directly and sequentially with one electrical contact point of said top metalization structure thereby creating a fan-out effect for said electrical contact point of said interconnecting metalization structure whereby the distance between said electrical contact points of said top metalization structure is larger than the distance between said electrical contact points of said interconnecting metalization structure by a measurable amount.

46. The method of claim 29 wherein said the number of said electrical contact pads of said upper metalization structure can be larger than the number of said contact points of said interconnecting metalization structure by a considerable and measurable amount.

47. The method of claim 29 wherein said metal conductors within said openings through said insulating layer and through said passivation layer connecting said electrical contact points of said top metalization structure with said contact points of said interconnecting metalization structure are constructed and routed such that each said electrical contact point of said interconnecting metalization structure is connected directly but not necessarily sequentially with one electrical contact point of said top metalization structure thereby creating a pad relocation effect for said electrical contact points of said interconnecting metalization structure whereby the distance between said electrical contact points of said top metalization structure is larger than the distance between said electrical contact point of said interconnecting metalization structure by a measurable amount whereby furthermore the sequence or adjacency of said electrical contact points of said interconnecting metalization structure is not necessarily the same as the sequence or adjacency between said electrical contact points of said top metalization structure.

48. The method of claim 29 wherein said metal conductors within said openings through said insulating layer and through said passivation layer connecting said electrical contact points on a top surface of said top metalization structure with contact

points of said interconnecting metalization structure are constructed and routed such that functionally identical electrical contact points of said interconnecting metalization structure are inter-connected and are connected with one electrical contact point or fewer electrical contact points of said top metalization structure thereby creating a reduction effect for said electrical contact points of said interconnecting metalization structure whereby the number of contact points for a particular electrical function within said electrical contact points of said top metalization structure is smaller than the number of said electrical contact points of said interconnecting metalization structure by a measurable amount whereby furthermore the sequence or adjacency of said electrical contact points of said interconnecting metalization structure is not necessarily the same as the sequence or adjacency between said electrical contact points of said top metalization structure.

49. A method for forming a top metalization system for high performance integrated circuits, comprising:
forming an integrated circuit comprising a plurality of devices formed in and on a semiconductor substrate, with an overlaying interconnecting metalization structure connected to said devices and comprising a plurality of first metal lines;

depositing an insulating, separating layer over said semiconductor substrate;

forming openings through said insulating, separating layer to expose upper metal portions of said interconnecting metalization structure;

depositing metal contacts in said openings; and

forming said top metalization system connected to said interconnecting metalization structure, wherein said top metalization system comprises a plurality of top metal lines, in one or more layers, having a width substantially greater than said first metal lines.

50. The method of claim 49 wherein said top metalization system comprises signal lines that are substantially wider than lines in said overlaying interconnecting metalization structure.

51. The method of claim 49 wherein said top metalization system comprises power buses that are substantially wider than lines in said interconnecting metalization structure.

52. The method of claim 49 wherein said top metalization system comprises ground buses that are substantially wider than lines in said interconnecting metalization structure.

53. The method of claim 49 wherein said top metalization system comprises planes that contain both signal lines and power buses that are substantially wider than lines in said interconnecting metalization structure.

54. The method of claim 49 wherein said top metalization system comprises planes that contain both signal lines and ground buses that are substantially wider than lines in said overlaying interconnecting metalization structure.

55. The method of claim 49 wherein said top metalization system comprises planes that contain both power buses and ground buses that are substantially wider than lines in said overlaying interconnecting metalization structure.

56. The method of claim 49 wherein said overlaying interconnecting metalization structure comprises electrical contact points whereby said contact points can comprise any appropriate contact material, such as but not limited to tungsten, copper (electroplated or electroless), aluminum, polysilicon, or the like.

57. The method of claim 56 wherein the size of said contact points is within the range of approximately 0.3 um. to 5.0 um.

58. The method of claim 49 further comprising depositing a passivation layer over said interconnecting metalization structure.

59. The method of claim 58 wherein said passivation layer comprises Plasma Enhanced CVD (PECVD) oxide.

60. The method of claim 58 wherein said passivation layer comprises Plasma Enhanced CVD (PECVD) nitride.

61. The method of claim 49 wherein said insulating, separating layer is a polymer dielectric layer or any other appropriate insulating material.

62. The method of claim 49 wherein said insulating, separating layer is selected from the group comprising polyimide and benzocyclobutene (BCB).

63. A method for forming a top metalization system for high performance integrated circuits, comprising: forming an integrated circuit comprising a plurality of devices formed in and on a semiconductor substrate, with an overlaying interconnecting metalization structure connected to said devices and comprising a plurality of fine-wire metal lines;

depositing a passivation layer over said interconnecting fine-wire metalization structure;

depositing an insulating, separating layer over said passivation layer that is substantially thicker than said passivation layer;

forming openings through said insulating, separating layer to expose upper metal portions of said overlaying interconnecting metalization structure;

depositing metal contacts in said openings thereby raising a plurality of contact points in said overlaying interconnecting metalization structure to the top surface of said insulating, separating layer thereby creating elevated interconnecting metalization contact points;

forming said top metalization system connected to said overlaying interconnecting metalization structure, wherein said top metalization system comprises a plurality of top wide-metal lines, in one or more layers, having a width substantially greater than said fine-wire metal lines, wherein said top metalization system directly interconnects said elevated interconnecting metalization contact points thereby functionally extending or connecting said fine-wire metal interconnects with said wide-wire metal interconnects thereby furthermore establishing electrical interconnects between multiple points within said fine-wire interconnects.

64. The method of claim 63 wherein said top metalization system comprises signal lines that are substantially wider than lines in said interconnecting metalization structure.

65. The method of claim 63 wherein said top metalization system comprises power planes that are substantially wider than lines in said interconnecting metalization structure.

66. The method of claim 63 wherein said top metalization system comprises ground planes that are substantially wider than lines in said interconnecting metalization structure.

67. The method of claim 63 wherein said passivation layer comprises Plasma Enhanced CVD (PECVD) oxide.

68. The method of claim 63 wherein said passivation layer comprises Plasma Enhanced CVD (PECVD) nitride.

69. The method of claim 63 wherein said insulating, separating layer is a polymer dielectric layer or any other appropriate insulating material.

70. The method of claim 63 wherein said insulating, separating layer comprises polyimide.

71. The method of claim 63 wherein said insulating, separating layer comprises the polymer benzocyclobutene (BCB).

72. The method of claim 63 wherein said insulating, separating layer is of a thickness after curing within the range of approximately 1.0 to 30 um.

73. The method of claim 63 wherein said insulating, separating layer is spin-on coated and cured.

74. The method of claim 63 wherein said openings have an aspect ratio within the range of approximately 1 to 10.

75. The method of claim 63 wherein said metal contacts is selected from the group comprising sputtered aluminum, CVD tungsten, CVD copper, electroplated copper, electroless nickel and damascene metal filling.

76. The method of claim 63 wherein said openings through said insulating, separating layer have sloped sides and wherein each of said openings is wider at its top.

77. The method of claim 63 thereby furthermore functionally and physically extending said top metalization system connected to

said overlaying interconnecting metalization structure, wherein said top metalization system comprises a plurality of ground planes, in one or more layers, wherein furthermore said overlaying interconnecting metalization structure directly interconnects a multiplicity of ground wires said ground wires to be connected with fine-wire ground wires thereby functionally extending or connecting said fine-wire ground wire metal interconnects with said wide-wire metal ground wire interconnects contained within said top metalization system thereby extending the fine-wire ground wires as contained within the overlaying interconnecting metalization structure with said top metalization system.

78. The method of claim 63 thereby furthermore functionally and physically extending said top metalization system connected to said overlaying interconnecting metalization structure, wherein said top metalization system comprises a plurality of signal planes, in one or more layers, wherein furthermore said overlaying interconnecting metalization structure directly interconnects a multiplicity of signal wires said signal wires to be connected with fine-wire signal wires thereby functionally extending or connecting said fine-wire signal wire metal interconnects with said wide-wire metal signal wire interconnects contained within said top metalization system thereby extending

the fine-wire signal wires as contained within the overlaying interconnecting metalization structure with said top metalization system.

79. The method of claim 63 thereby furthermore functionally and physically extending said top metalization system connected to said overlaying interconnecting metalization structure, wherein said top metalization system comprises a plurality of power planes, in one or more layers, wherein furthermore said overlaying interconnecting metalization structure directly interconnects a multiplicity of power wires said power wires to be connected with fine-wire power wires thereby functionally extending or connecting said fine-wire power wire metal interconnects with said wide-wire metal power wire interconnects contained within said top metalization system thereby extending the fine-wire power wires as contained within the overlaying interconnecting metalization structure with said top metalization system.